FIG. 3A, the method utilizes a conventionally processed semiconductor wafer 300 that has a top surface 310. Surface 310, in turn, has a number of substantially-equal lower levels 312 and a number of substantially-equal upper levels 314 that lie above the lower levels 312.

The first paragraph on page 5 has been amended to read as follows:

As further shown in FIG. 3A, the method begins by depositing a layer of polysilicon 320 on surface 310. Polysilicon layer 320 is conformally deposited and, as a result, also has a top surface 321 that has a number of substantially-equal lower levels 322 and a number of substantially-equal upper levels 324 that lie above the lower levels 322.

The fifth paragraph on page 5 (which continues on to ~~page~~ 6) has been amended to read as follows:

Alternately, after the planarization step, one or more additional layers of materials, such as materials which lower the resistance of polysilicon, can be formed over layer 340. As shown in FIG. 3C, a layer of material 342 that lowers resistance is formed over planarized polysilicon layer 340. The mask is then formed and patterned on the additional layers of material (e.g., layer 342) which are then etched along with planarized polysilicon layer 340 to form the structures (e.g., local interconnect lines). Either way, once the structures have been formed, the method continues with conventional back-end processing steps.

In the Claims

Please cancel claims 3, 4, 8, 11, and 12.

Please amend the claims as follows:

1. (Amended) A method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of: